ABSTRACT OF THE DISCLOSURE

The semiconductor storage device comprises memory cell transistors formed on a semiconductor substrate 10; first insulation films 42 covering the top surfaces and the side surfaces of gate electrodes 20 of the memory cell transistors; through-holes 40 opened on first diffused layers 24; a second insulation film 36 with through-holes 40 opened on first diffused layers 24 and through-holes 38 opened on second diffused layers 26 formed in; capacitors formed on the inside walls and the bottoms of the through-holes 40 and including capacitor storage electrodes 46, connected to the first diffused layers 24; capacitor dielectric films 48 covering the capacitor storage electrodes 46, and capacitor-opposed electrodes 54 covering at least a part of the capacitor dielectric films 48; and, contact conducting films 44 formed on the inside walls and bottoms of the through-holes 38, and connected to the second diffused layers. This structure of the semiconductor storage device makes it unnecessary to secure an alignment allowance for alignment of the through-holes 40 opened on the first diffused layer 24 and the through-holes 38 opened on the second diffused layer 26 with the gate electrode 20, which permits the semiconductor storage device to have a small memory cell area.